AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 15, 21 and 22 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

an analog circuit configured to generate a plurality of samples of an input signal in response to a plurality of phases of a reference clock; and

a digital circuit configured to generate an output signal and a clock signal in response to said plurality of samples and said plurality of phases, wherein (a) said clock signal is aligned with said output signal and (b) said digital circuit comprises a synchronization circuit comprising (i) a first stage configured to generate a first intermediate output in response to said plurality of samples and said plurality of phases, (ii) a second stage configured to generate a second intermediate output in response to a first portion of said first intermediate output and one of said plurality of phases and (iii) a third stage configured to generate a plurality of synchronized data signals in response to a second portion of said first intermediate output and said second intermediate output in response to a second one of said plurality of phases.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said analog circuit comprises:

a plurality of comparators, each configured to generate a logic level output in response to a reference signal and one of said plurality of samples of said input signal; and

a plurality of pass gates, each configured to present said one of said plurality of samples of said input signal in response to one of said plurality of phases of said reference clock.

3. (ORIGINAL) The apparatus according to claim 1, wherein said analog circuit comprises a multi-phase phase locked loop circuit configured to generate said plurality of phases.

4. (ORIGINAL) The apparatus according to claim 1, wherein said clock signal is aligned with a predetermined point of a bit time of said output signal.

5. (ORIGINAL) The apparatus according to claim 1, wherein said clock signal is aligned with a center of a bit time of said output signal.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said digital circuit comprises one or more output

circuits selected from the group consisting of (i) a serial output circuit configured to generate a serial data signal and a serial clock signal, (ii) a packed data output circuit configured to generate a packed data signal and a first strobe signal, and (iii) a symbol data output circuit configured to generate a symbol data signal, a polarity signal and a second strobe signal.

7. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said digital circuit is configured to align said clock signal by selecting one of said plurality of phases in response to ~~an~~ a first accumulated value.

8. (CURRENTLY AMENDED) The apparatus according to claim 7, wherein said digital circuit is configured to increment said first accumulated value by a calculated bit width each time a phase is selected.

9. (ORIGINAL) The apparatus according to claim 7, wherein said digital circuit is configured to align said clock signal by selecting another one of said plurality of phases in response to a second accumulated value.

10. (ORIGINAL) The apparatus according to claim 9, wherein said digital circuit is configured to increment said first

and second accumulated values by a calculated bit width each time a phase is selected.

11. (ORIGINAL) The apparatus according to claim 9, wherein said digital circuit is configured to generate said clock signal having two edges within a period of a predetermined one of said plurality of phases.

12. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein said digital circuit is configured to determine a period of said clock signal based on a calculated bit width.

13. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said output signal comprises one or more signals selected from the group consisting of a serial data signal, a packed data signal, a symbol data signal, a polarity signal and a strobe signal.

14. (ORIGINAL) The apparatus according to claim 6, wherein said serial output circuit comprises a first-in-first-out (FIFO) memory having no resynchronization logic.

15. (CANCELED)

16. (CURRENTLY AMENDED) A method for extracting ~~clock and~~ data information from an input signal comprising the steps of:

(A) receiving said input signal;

(B) generating a plurality of ~~analog~~ samples of said input signal in response to a plurality of phases of a reference clock; ~~and~~

(C) generating an output signal and a clock signal in response to said plurality of ~~analog~~ samples, a reference signal and said plurality of phases, wherein said clock signal is aligned with said output signal;

(D) generating a first intermediate output in response to said plurality of samples and said plurality of phases;

(E) generating a second intermediate output in response to a first portion of said first intermediate output and one of said plurality of phases; and

(F) generating a plurality of synchronized data signals in response to a second portion of said first intermediate output and said second intermediate output in response to a second one of said plurality of phases.

17. (CURRENTLY AMENDED) The method according to claim 16, wherein step (B) comprises the sub-step of:

sampling said input signal with a plurality of sample and hold gates controlled by said plurality of phases of said reference clock to generate said plurality of samples.

18. (CURRENTLY AMENDED) The method according to claim 17, wherein step (C) further comprises the sub-step of:

selecting one of said plurality of phases as said clock signal in response to ~~an~~ a first accumulated value.

19. (ORIGINAL) The method according to claim 18, wherein step (C) further comprises the sub-step of:

selecting another of said plurality of phases as said clock signal in response to a second accumulated value.

20. (PREVIOUSLY PRESENTED) The method according to claim 19, wherein step (C) further comprises the sub-steps of:

decrementing said first and said second accumulated values by the number of phases in said plurality of phases; and

incrementing said first and said second accumulated values by a calculated bit width.

21. (CANCELED)

22. (CANCELED)

23. (CURRENTLY AMENDED) The apparatus according to claim ~~22~~24, wherein said symbol width determining circuit comprises:

a data width counter configured to generate said first strobe signal, said second strobe signal and a data width signal in response to said plurality of synchronized data signals;

a symbol width correction logic configured to generate said high data signal and said low data signal in response to said data width signal, a width comparison signal and a lock detection signal;

a width comparison circuit configured to generate said width comparison signal, a high bit signal and a low bit signal in response to a first table value selected in response to said first strobe signal and said high data signal and a second table value selected in response to said second strobe signal and said low data signal; and

a bit width calculation circuit configured to generate said lock detection signal and said calculated bit width signal in response to said high bit signal and said low bit signal.

24. (NEW) An apparatus comprising:

an analog circuit configured to generate a plurality of samples of an input signal in response to a plurality of phases of a reference clock; and

a digital circuit configured to generate an output signal and a clock signal in response to said plurality of samples and said plurality of phases, wherein (a) said clock signal is aligned with said output signal and (b) said digital circuit comprises (i) a synchronization circuit configured to generate a plurality of synchronized data signals in response to said plurality of samples of said input signal and said plurality of phases of said reference clock and (ii) a symbol width determining circuit configured to generate a first strobe signal, a second strobe signal, a high data signal, a low data signal and a calculated bit width signal in response to said plurality of synchronized data signals.